What is claimed is:

1. A method of fabricating a metal interconnection of semiconductor device comprising the steps of:

depositing a metal layer on a substrate having a predetermined structure;

patterning a bottom metal layer by etching the metal layer;

forming a pad electrically connecting the bottom metal layer to a scribe area;

forming an insulating layer on the substrate including the bottom metal layer;

forming a via hole and a trench, in which an upper metal layer is formed, on the insulating layer, the via hole connecting the bottom metal layer with the upper metal layer;

forming a plating layer by means of electroplating; and

performing a planarization process for the plating layer.

2. The method as defined by claim 1, further comprising a step of forming a barrier metal layer prior to the formation of the plating layer.

3. The method as defined by claim 1, wherein the insulating layer is a TEOS layer deposited by PECVD.

4. The method as defined by claim 2, wherein the barrier metal layer is a single layer that is made of a metal selected from the group of Ta, TaN, TaAlN, TaSiN, $TaSi_2$, Ti, TiN, TiSiN, WN, Co, and $CoSi_2$, or a multi-layer that is made of at least two metals selected from said group.

5. The method as defined by claim 1, wherein the plating layer is a copper layer.

6. The method as defined by claim 1, wherein the electroplating comprises the steps of:

loading the substrate into a chamber where electroplating process is performed;

applying a voltage using the substrate as a cathode; and

forming a plating layer by immersing the substrate in an electrolyte.

7. The method as defined by claim 6, wherein the voltage is applied through the pad formed in the scribe area.

8. The method as defined by claim 1, wherein the planarization process is a CMP process.

9. The method as defined by claim 8, wherein the CMP process is performed for the plating layer until the surface of the insulating layer is exposed.